

國家科學及技術委員會 函

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主旨：本會公開徵求115年度「晶創計畫：次世代半導體材料與元件整合關鍵技術」計畫書，自即日起受理申請，請於115年2月26日前依徵求公告規定，檢附相關文件備函提出申請，逾期恕不受理，請查照轉知。

說明：

一、本計畫徵求公告請詳閱附件，亦可至本會網站之計畫徵求專區或自然科學及永續研究發展處公告網頁下載。

二、研究計畫申請書請依本會補助專題研究計畫作業要點之規定辦理；線上申請作業時，請選擇「專題類—隨到隨審計畫」，計畫類別為「一般策略專案計畫」，研究型別為「整合型計畫」，計畫歸屬為「自然處」，學門代碼請勾選「M9201—前瞻半導體」。

三、申請案依規定程序進行審查，並依審查結果及經費預算擇優補助；未獲補助案件恕不受理申覆。

四、本案相關聯絡資訊：

(一)申請內容疑義：請洽本會自然處郭廷洋助理研究員，電

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正本：專題研究計畫受補助單位（共253單位）

副本：本會綜合規劃處、自然處(均含附件)

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國科會自然處

115 年度「晶創計畫：次世代半導體材料與元件整合關鍵技術」 計畫徵求公告

壹、計畫背景及目的

隨著傳統 CMOS 技術逐漸逼近微縮極限，全球半導體研究正加速朝 Beyond CMOS 與新型材料技術發展。大面積新興半導體材料在能帶調控、界面行為與新型元件架構上具有高度潛力，但在大面積材料生長品質、製程相容性、電性穩定度與鑑測能力等面向，仍存在待突破的科學與技術挑戰。國內產業在新材料導入、先進製程驗證與元件評估方面亦有方法與流程上的不足，需強化基礎科學與研究工具，以支援未來產業技術發展。

本計畫「晶創計畫：次世代半導體材料與元件整合關鍵技術」旨在建立次世代半導體材料與元件所需的核心研究能量，支持學術界就材料生長、材料行為、製程整合、元件操作及鑑測方法提出創新研究構想，建構材料-製程-元件與驗證的鏈結，補足現階段研究端與產業端在材料理解、製程評估與鑑測方法上的缺口。

藉由推動跨領域合作與實作驗證，本計畫期望建立研究端與產業端可連結的技術基礎，支援未來新興材料或新元件架構的導入評估，並強化我國於 Beyond CMOS 與次世代半導體領域的長期研發競爭力。

貳、計畫研發方向

本計畫以開放式研究方向徵求具創新的學術構想，聚焦於次世代半導體材料與元件行為的核心科學議題，並補強目前產業在材料特性掌握與鑑測技術上的關鍵缺口。研究方向強調基礎研究與未來先進製程需求的連結，鼓勵提出有助於新材料或新元件長期路線探索的研究設計，以支援 Beyond CMOS 技術之布局。研究範疇可大致分為二大主軸：

一、半導體材料、製程與元件行為之研究：聚焦於大面積半導體及二維材料在不同製程條件、環境或元件架構下所展現的行為與效應，並兼顧科學

原理、應用需求與實作驗證。研究內容可涵蓋材料生長與結構調控、界面與能帶特性、載子傳輸行為、元件操作機制，以及在先進製程條件下的穩定性、相容性或電性表現等議題。鼓勵提出能連結材料特性、製程開發與元件操作的整合型研究構想，從科學理解延伸至製程驗證、原型元件製作或效能評估，以建立未來新材料或新架構導入先進製程時所需的基本資料與可行性依據。

二、跨尺度量測、鑑測技術與資料分析方法：著重於強化半導體材料與元件在結構、界面、缺陷與操作行為等面向的量測與鑑測能力，並提升相關方法在產業實務中的適用性。鼓勵發展可支援先進製程需求的量測與驗證流程，例如具備較高穩定度、再現性、效率或製程相容性的方法。亦鼓勵結合理論模型、模擬或資料分析工具，以協助量測結果的判讀速度與可靠度提升，提供材料特性、製程影響與元件行為之整體評估，並作為後續技術開發的重要參考。

參、計畫內容撰寫說明

本計畫採目標導向之徵求方式，申請內容應清楚呈現研究構想、技術重點與可行性，並兼顧科學探索、製程實作與未來發展之連結。

一、研究目標與核心問題：說明計畫所欲探討的主要科學或技術議題，包括材料行為、製程效應、元件操作或量測能力等面向。鼓勵提出具前瞻性與創新性的研究構想，並說明對次世代半導體技術之可能貢獻。

二、研究規劃與技術藍圖：提出具體之三年期研究規劃，包括研究主軸、預期成果、階段目標及驗證方式。規劃可涵蓋材料特性理解、製程整合探索、元件實作或新型量測方法等，並可視研究特性提出多種可能之進行路徑，以反映研究的不確定性與彈性。

三、研究定位與指標設定：說明本研究在國內外技術發展中的定位，包括其對 Beyond CMOS、先進材料、製程技術或新型元件架構的關聯性。並提出可作為研究進展評估之量化或質性指標，如材料品質、製程行為、元件表現或量測能力提升等。若涉及跨領域合作或複雜製程路線，可敘述

不同研究策略的分工與評估方式。

四、產業需求與後續應用潛力：說明未來先進製程、量測技術或元件開發中的可能應用場景，並可敘述如何回應目前產業在材料導入、製程相容性或鑑測方法上的需求。若研究包含材料或元件實作、流程開發或更貼近製程環境之量測方法，建議說明其可行性、穩定度與實務價值。

肆、計畫及構想書申請、審查及核定

一、申請須知：申請機構與計畫主持人須符合本會「補助專題研究計畫作業要點」之規定。本專案以申請分年多年期之單一整合型研究計畫為原則。整合型計畫以 2 至 4 個子計畫為宜（含總主持人 1 件）。各子計畫主持人應具實質研究角色，計畫書須清楚敘述各子計畫之主題分工與整合方式，並說明整體計畫目標與預期成果。研究計畫每年經費規模以 500–2000 萬元為原則，實際補助金額將依審查結果及預算狀況核定。

二、申請程序：本專案採單階段完整計畫書審查方式。申請人應依本會線上申請系統完成資料填寫及上傳作業，由申請機構於期限內送件，申請人之任職機構應於 115 年 2 月 26 日(星期四)前備函送達本會(請彙整造冊後專案函送，逾期恕不受理)。計畫書內容須依「專題研究計畫申請書表 CM03」之格式與頁數規範撰寫。

線上申請時，請選擇「專題類—隨到隨審計畫」，計畫類別為「一般策略專案計畫」，研究型別為「整合型計畫」，計畫歸屬為「自然處」。學門代碼請勾選「M9201—前瞻半導體」，子學門代碼則依研究內容擇定為「M920102—前瞻半導體—關鍵元件材料」或「M920101—前瞻半導體—檢測技術」。

三、審查與核定：審查方式包括書面初審及會議複審。本計畫屬專案計畫，審查未獲通過者，恕無申覆機制。本計畫以三年期為原則，經核定後列為分年多年期計畫，每年將依執行成效考評結果決定次年度之續辦與補助情形。計畫核定後列入總主持人之計畫件數管理；子計畫主持人不列入計畫件數。總主持人及子計畫主持人，得核給研究主持費最高每個月

新台幣 30,000 元及 20,000 元，於計畫執行期間僅得支領 1 份研究主持費，同一執行期限若同時執行 2 件以上，以最高額度計算，並得於不同計畫內採差額方式核給。

四、審查重點：審查將整體考量學術價值、技術可行性、研究整合度及與本專案目的之契合度，重點包括：

- (1) 計畫提案的企圖心、技術前瞻性與挑戰性。
- (2) 與全球半導體技術發展之契合度。
- (3) 研究內容之新穎性、技術突破潛力與科學貢獻。
- (4) 研究成果對先進製程、材料開發或量測方法之應用與落地可行性。
- (5) 技術藍圖與量化指標設定的明確性與合理性。
- (6) 計畫主持人及團隊之執行能力與研究能量。
- (7) 團隊成員之跨領域整合能力與產學合作之潛力。

伍、執行與考評

一、本會將對執行計畫定期進行考評，執行團隊須配合提供計畫執行進度與成果，並出席相關審查會議。考評結果將作為次年度經費核定與計畫續辦之重要依據。

二、執行團隊須配合本會辦理計畫執行成果發表、推廣應用及交流等相關事宜。各年度所需經費如未獲立法院審議通過或經部分刪減，國科會得依實際情形調整補助經費。如未依規定繳交報告，或執行成效未如預期且未能改善時，本會得調減次年度經費或終止該計畫。

陸、其他注意事項

一、本計畫之簽約、撥款、延期與變更、經費結報及報告繳交等，應依本會補助專題研究計畫作業要點、補助專題研究計畫經費處理原則、專題研究計畫補助合約書與執行同意書及其他有關規定辦理。

二、公告未盡事宜，應依本會補助專題研究計畫作業要點、本會補助專題研究計畫經費處理原則及其他相關法令規定辦理。

柒、計畫聯絡方式

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National Science and Technology Council (NSTC) Call for Proposals

Taiwan Chip-based Industrial Innovation Program (Taiwan CbI): Key Technologies for Integrating Next-Generation Semiconductor Materials and Devices FY2026-2028

1. Background and Objectives

As conventional CMOS technologies approach scaling limits, global semiconductor research is shifting toward Beyond-CMOS concepts and emerging materials. Large-area semiconductor materials offer significant potential in band engineering, interfacial behavior, and novel device architectures. However, challenges remain in achieving high-quality large-area growth, ensuring process compatibility, maintaining electrical stability, and establishing robust metrology. Domestic industry likewise faces gaps in materials introduction, advanced process verification, and device evaluation.

The Taiwan Chip-based Industrial Innovation Program (Taiwan CbI) aims to establish core research capabilities for next-generation semiconductor materials and device integration. The program supports academic research on materials growth and behavior, process integration, device operation, and metrology development, thereby connecting materials–process–device–validation workflows. Through interdisciplinary collaboration and experimental verification, this program seeks to establish a research foundation that aligns with industrial needs and enhances long-term competitiveness in Beyond-CMOS and next-generation semiconductor technologies.

2. Research Themes

The program solicits innovative academic proposals within open research directions centered on fundamental questions of materials behavior and device

operation, while addressing key metrology and process-related gaps relevant to future manufacturing. Proposals should connect fundamental science with anticipated industrial requirements and contribute to long-term exploration of new materials or device architectures. The program encompasses two major themes:

- I. Semiconductor Materials, Process Integration, and Device Behavior:** Research focuses on large-area semiconductor and 2D materials under diverse process conditions, environmental settings, or device architectures. Topics include: materials growth and structural control, interfacial and band structure characteristics, carrier transport mechanisms, device operation physics, stability, compatibility, and electrical performance under advanced process conditions. Proposals are encouraged to integrate materials science, process development, and device operation, extending from fundamental understanding to process validation, prototype device fabrication, or performance assessment. Outputs should support feasibility evaluation for incorporating new materials or architectures into future advanced processes.
- II. Multi-Scale Characterization, Metrology, and Data Analytics:** This theme emphasizes strengthening characterization capabilities across structure, interface, defects, and device operation. The program encourages the development of metrology workflows that meet industrial relevance with improved stability, reproducibility, throughput, or process compatibility. The integration of theoretical modeling, simulation, or data analytics is also supported to enhance the speed and reliability of data interpretation, facilitating a comprehensive assessment of materials properties, process influences, and device behavior.

3. Proposal Preparation Guidelines

This call is goal-oriented. Proposals must clearly articulate the research concept, technical focus, feasibility, and the linkage between scientific exploration, process implementation, and downstream applications.

- I. Research Objectives and Core Questions: Define the key scientific or technological issues to be addressed, such as materials behavior, process effects, device operation, or metrology capabilities. The proposal should demonstrate forward-looking and innovative ideas and their potential contributions to next-generation semiconductor technologies.
- II. Research Plan and Technical Roadmap: Provide a three-year research plan describing major research thrusts, expected outcomes, milestones, and validation methods. Plans may involve materials characterization, process integration studies, device prototypes, or new metrology approaches. Multiple research paths may be proposed to reflect uncertainties and allow flexibility.
- III. Positioning and Performance Indicators: Explain the proposal's position within domestic and international technological developments, including its relevance to Beyond-CMOS materials, process technologies, or novel device architectures. Present quantitative or qualitative indicators for assessing research progress, such as materials quality, process behavior, device performance, or metrology capability. For interdisciplinary or complex process-related work, describe team roles and assessment methods.
- IV. Industrial Needs and Application Potential: Discuss potential applications in advanced processing, metrology, or device development. Explain how the research addresses current industrial needs in materials introduction, process compatibility, or metrology methods. If the work involves prototype development or process-relevant workflows, describe feasibility, expected stability, and practical value.

4. Application, Review, and Funding

- I. Eligibility and Funding Structure: Applicants must comply with NSTC regulations on project funding. The program adopts a single integrated project structure, typically comprising of 2–4 sub-projects led by an overall PI. Each sub-project PI must have a substantive research role. The proposal should clearly describe

responsibilities and integration mechanisms across sub-projects. Annual funding is expected to range from NT\$5 million to NT\$20 million, with final amounts determined by review results and budget availability.

- II. Submission Procedure: Submit the full proposal through the NSTC online system using the required templates. The proposal must follow the format and page limits of the NSTC CM03 Proposal Form. In the online system, select: Project Type: Research Projects – Rolling Review. Program Category: Strategic Program. Research Type: Integrated Project. NSTC Division: NSTC Department of Natural Sciences and Sustainable Development. Discipline Code: M9201 – Advanced Semiconductors. Sub-discipline Code: choose M920102 – Key Component Materials or M920101 – Metrology Technologies, depending on research content.
- III. Review and Funding Decision: Review consists of preliminary written evaluation followed by a panel meeting. As a strategic program, decisions are final and no appeal mechanism is provided. Projects are funded for three years in principle. Continuation each year depends on performance evaluations. After approval, the project counts toward the PI's project quota; sub-project PIs are not counted. PI and sub-project PIs may receive a monthly PI allowance of up to NT\$30,000 and NT\$20,000, respectively, with only one allowance claimable at a time.
- IV. Review Criteria: Evaluation considers academic merit, technical feasibility, integration quality, and alignment with program objectives. Key criteria include:
 - (1) Ambition, forward-looking vision, and technical challenge.
 - (2) Relevance to global semiconductor development trends.
 - (3) Novelty, potential for breakthroughs, and scientific contributions.
 - (4) Applicability to advanced processing, materials development, or metrology.
 - (5) Clarity and appropriateness of the technical roadmap and performance indicators.
 - (6) Execution capability of the PI and team.
 - (7) Interdisciplinary integration and potential for academia-industry

collaboration.

V. Project Implementation and Evaluation

NSTC will conduct periodic evaluations. Teams must provide progress reports and attend review meetings. Evaluation results directly influence the following year's funding and continuation decisions.

Teams must also participate in dissemination activities, technology promotion, and related NSTC-designated events. If annual budgets are not approved by the Legislative Yuan or are partially reduced, NSTC may adjust funding accordingly. Projects may be reduced or terminated for failure to comply with reporting requirements or inadequate performance.

VI. Additional Provisions

Contracting, fund disbursement, extensions, amendments, financial reporting, and submission of deliverables must comply with the NSTC Regulations on Research Project Grants, related financial principles, and relevant laws. Unspecified matters will follow the same regulations.

VII. Contact Information

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For system operation issues, please contact the NSTC Information System Service

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